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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/759,855	01/16/2004	Tien-Chun Yang	0180185	8750

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EXAMINER	
WELLS, KENNETH B	
ART UNIT	**PAPER NUMBER**
2816	

DATE MAILED: 08/16/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/759,855	YANG ET AL.	
	Examiner	Art Unit	
	Kenneth B. Wells	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3 and 5-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,5,6,8-12 and 14-19* is/are rejected.

7)☒ Claim(s) *7,13 and 20* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. In view of newly discovered prior art, the previous indication of allowability of the claims is hereby withdrawn and a new prior art rejection is set forth below. Any inconvenience caused by the delay in citing this new prior art is regretted.

2. Claim 10 is objected to because of the following informalities: in claim 10, "said intrinsic FET means" lacks clear antecedent basis. Appropriate correction is required.

3. Claims 1-3, 5, 6, 8-12 and 14-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Uekubo in view of any one of Mizuno et al '374, Mizuno et al '360, Hidaka et al '222, Hidaka et al '986, Morishita, Schneider et al and Kawahara et al.

Note Fig. 2 of Uekubo, which shows a cascode amplifier circuit 100, where the recited first through fourth FETs read on FETs 213, 215, 212 and 216, respectively; the recited "target memory cell" reads on memory cell 102; the recited "bit line" reads on the wire connection between cell 102 and amplifier circuit 100. Also note reference voltage ground to whoch the sources of FETs 213, 215 are

directly connected. Not disclosed by Uekubo is that the first through third FETs are "intrinsic", defined by applicant as a low threshold FET with Vt in the range from 0.3V to 0.5V. Such would have been obvious to those having ordinary skill in the art because it is notoriously well-known in the art that the switching speed of an amplifier circuit can be enhanced simply by lowering the Vt values of the FETs included therein (see the several secondary references for such a teaching). Lowering the Vt values of all the FETs in Fig. 2 of Uekubo so that Vt is anywhere from 0.3V to 0.5V (known in the art to be lowered Vt, since 0.7V is the typical Vt of a FET) is therefore suggested by each of the several secondary references.

As to claims 3, 10 and 16, the recited W/L ratio is deemed to be an obvious design expedient, i.e., the skilled artisan would easily recognize that the W/L ratios of the various FETs in Fig. 2 of Uekubo can be set to any values, depending simply on the desired operating characteristics of the circuitry. Thus, claims 3, 10 and 16 also do not define patentably over Uekubo.

As to claim 17, note that the input control voltage SAE 130 controls whether or not the bit line (path through FET 106) is activated, which is broadly interpreted as a

type of "correspondence", thus meeting the language of this claim as well.

4. Claims 7, 13 and 20 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Note the further references cited on the attached PTO-892 which are further examples teaching the relationship between lowering the Vt value of a FET to thereby achieve faster switching speed.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kenneth B. Wells whose telephone number is (571)272-1757. The examiner can normally be reached on Monday through Friday from 8:30am to 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy P. Callahan, can be reached at (571)272-1740. The fax phone

number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Kenneth B. Wells
Primary Examiner
Art Unit 2816

August 4, 2005